Challenges of Leadframe-Based Micro-Packages

While micro-packages may not boast hundreds of I/Os or garner the lion's share of attention in the semiconductor packaging market, they represent a package type that is produced in the billions annually, and is every bit as demanding in its production requirements as the denser, more "exotic" packages.

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Packing the maximum circuit functions at the optimum performance in the smallest PWB space at the lowest overall cost continues to be a major driver in semiconductor packaging technology.

The demand for smaller, thinner, faster, cooler and more reliable packages is an evolutionary process that constantly adapts to changing requirements.

Industry literature tends to focus on the "sexy" technology associated with high pincount ball-grid array packages used for microprocessors, 3D packages or System-in-Package.

Demanding Technologies

Meanwhile, there has been little discussion about the demanding technologies associated with micro-packages that represent the great majority of the billions of packages produced every year.

The general perception is that leadframe-based, micro-packages with pincounts of 10 or less are low technology; this could not be farther from reality.

The technology challenges associated with manufacturing a package with six I/Os that is as small as the font size used for the type in this article is every bit as demanding as many of the other "perceived" advanced technology packages. (Figure 1 shows some micro-package examples.).

A technician conducts pilot packaging research at a Carsem plant.

Semiconductor packages possess a huge range of sizes and a wide variety of performance demands that depend on the electrical functions of the semiconductor die housed inside.

At one end of the size spectrum, large packages used for microprocessors and graphics chips are greater than 30mm x 30mm with I/O counts in the thousands.

An example of a micro-package at the small end of the spectrum is an MLP (Micro Leadframe Package) that is only 2mm x 1mm with 5 I/Os as shown in Figure 1. Regardless of size, the basic assembly process shown in Figure 2 is common to all sizes.

Major Challenges

This article discusses some of the major challenges associated with the assembly process used in the high-volume manufacturing of leadframe-based micro-packages.

Keep in mind that the volumes of a single micro-package produced at just one packaging foundry may easily run **over one million units per day**. As a result, some of these challenges are magnified by the need for extremely high throughput rates at very low cost.

Wafer Saw

Die sizes used in micro-packages are very small; it is quite common for one 200mm wafer to contain over 75,000 die and require more than 90 minutes to saw.

Even at this high die count, there is a

Figure 1. Left to right is a bottom view of a 3-lead SOT-883 (Mini-MLP), 6-lead SOT-666, 5-lead 2x1mm MLP, 8-lead SC70, and an 8-lead 2x2mm MLP.

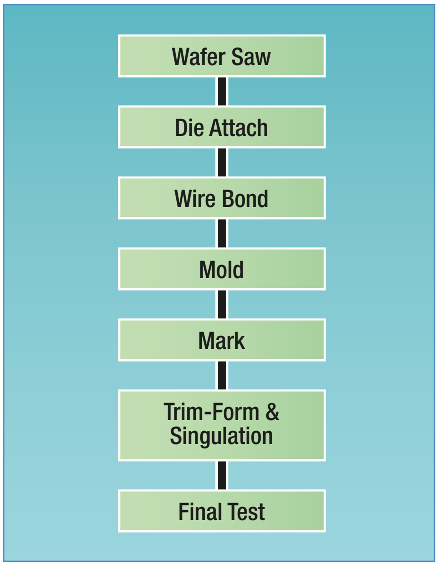

Figure 2. The basic assembly process flow for plastic packages

drive to reduce the saw street widths and place wafer-fab test site monitors in the saw streets to increase die density further. In addition, the need for thinner micro-packages is driving the industry to backgrind wafers to thinner and thinner geometries.

Some major challenges associated with the wafer saw process for micro-package devices are:

- **Dust Buildup**—Considering the amount of time is takes to saw a single wafer, it is a major challenge to keep the large amount of saw "dust" generated to an absolute minimum. If the dust is not properly controlled, the dust particulates will land and stick to the die surface causing reliability and quality problems.
- **Overheated Saw Blades**—Special methods for cooling the saw blade are required to keep it from overheating, which helps eliminate die chipping, reduces saw dust, extends the life of the blade and lowers the risk of a blade failure while sawing a wafer.
- **Backside Die Chipping**—It is a significant task to develop a saw process that will optimize throughput, while reducing cost and eliminating any backside die chipping. Unlike larger die sizes, a 2-mil backside chipout is not acceptable.

Die Attach

Many of the die sizes for micro-packages range from 10 to 30 mils. To keep material costs low, the leadframe strips are in a large matrix format and die-attach machines are designed for high throughput rates.

However, the need to meet moisture sensitivity levels (MSL) at 260°C has resulted in development of higher "filler" content in the newer generation die-attach epoxies. This, in turn, has created epoxy dot-size dispensing issues that may compromise throughput. To squeeze the largest possible die into a given package, leadframe designers are pushing the limits for the largest die-attach paddle possible; therefore, die placement accuracy is extremely critical.

Some challenges associated with the die-attach process for micro-packages are:

- **Epoxy Dispense Tolerances**—Tight control of a very small die-attach epoxy dot size and thickness is far more critical when compared to die sizes in larger packages.

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- **Epoxy Dispense Speeds**—High-speed epoxy dispensing with tightly controlled pressure and closed-loop feedback systems is critical to maintain consistent quality of the attached die.
- **Die Placement Tolerances**—Highly accurate die placement in the range of plus or minus 1.5 mil. and 2° rotation—trending to even less—at high productivity rates is essential. Precise die placement is required to provide exact wire bond lengths, especially for RF devices.

Wire Bond

The need to minimize die size to lower overall cost is pushing designers to smaller and smaller bond-pad sizes and finer pitches.

In many cases, fine-pitch wire bond issues for micro packages with I/O counts as low as 5 pads are similar to larger die with high I/O counts.

Many of the micro-packages are used for MOSFET devices, where *RDSon* is critical, so the need for using multiple wires, large-wire diameters and copper wire is a significant burden.

Flip-chip technology, similar to that used for large array packages, is also employed in micro-package production.

Some major challenges for the wire bond process used for micro-packages are:

- **Low Wire Loops**—Low wire loops are required for new generation micro-packages that are less than 0.5mm thick, because there is very little vertical space to the top of the package.

  Micro-package devices are very cost competitive, and most of the alternatives for thinning the die are expensive, making low-wire loop height the most cost-effective solution.
- **Multiple Large-Diameter Wires**—Putting the maximum number of larger-diameter wires on bond pad areas without causing cratering under the pad is a significant task. The shift to copper wire to reduce costs and enhance performance is another significant area.
- **RF Demands**—Micro-packages used for RF devices often require a large number of down-bonds to the die attach pad. These down-bonds provide a grounding effect that reduces noise.

Mold

There are two general categories for molding leadframe-based packages. One is an individual cavity mold, where the package is produced by molding individual die sites on the leadframe strip. Sing-

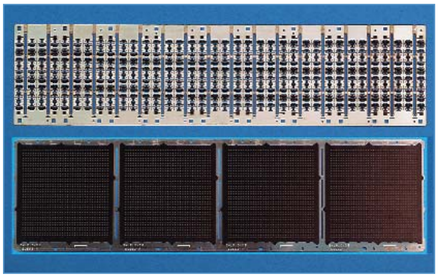

Figure 3. At top is an SOT-666 molded strip with 288 mold cavities; at bottom is a SOT-883 (Mini-MLP) array molded strip with 7140 units.

ulation is accomplished via a mechanical punch.

The other molding category is an array mold, where a large area of the leadframe strip containing multiple die sites is overmolded and then singulated with a saw. (Figure 3 shows an example of each type.)

Some leadframe strips used in cavity molds may contain over 780 parts, and the associated mold chase holds two strips with over 1560 cavities.

Because micro-packages are so small, they cannot be ejected from the mold by using ejector pins that push on the package body; this method is employed for larger packages.

In array molds, some leadframe strips contain over 7100 parts, and the associated mold press can hold two strips; one mold shot may contain more than 14,000 units. Due to problems of warping caused by the mismatch of the CTE of the copper leadframe and the molding compound, the entire area of the strip should not be molded and must be limited to a maximum area of about 52mm x 52mm, as shown in Figure 3.

The new generation of "green" mold compounds have a greater tendency to stick when very large mold areas are involved.

Marking

Micro-package marking is a far greater challenge than with larger packages. One example is the requirement to print three characters on a SOT-883 (3-lead 1.0mm x 0.6mm Mini-MLP). This package requires laser marking, which adds an additional concern related to the depth of the marking needed to avoid damaging the wire bond.

Trim-Form and Singulation

There are two types of packages used in this assembly step. One is a package with "formed leads" that are mechanically singulated, and the other is a leadless package, such as an MLP, that is saw-sinsingulated. (Some options are mechanically singulated.)

Because micro-packages are so small, the package designer must do everything possible to accommodate the largest possible die.

To accomplish mechanical form and singulation of leaded packages, the package body must be as large as possible, which makes the trimming and forming of the leads a significant concern.

In addition, the draft angle of the body must be as shallow as possible without causing mold-release problems. (See Figure 4, which compares a SOT-23 micro-package with an MSOP.)

Alternatively, saw-singulated micro-packages typically require etched leadframes with extremely tight tolerances. The sawing equipment needs to have highly accurate pattern recognition and precision indexing capability.

The difficulty of sawing is compounded by the fact that the tape, to which the leadframe strips are mounted for the sawing process, expands during the process due to the multitude of cuts made while sawing.

Many of the saw-singulated packages have the leads exposed on the bottom. This condition requires specially designed leadframe features to enhance the saw process, avoid creating metal burrs and eliminate chipping of the plastic body.

Test Socketing

One significant challenge is to insert the micro-package into the test socket in the correct orientation, and make good, consistent electrical contact.

An example of a package requiring extra care is the 2mm x 2mm MLP with 8 leads (seen in Figure 1), where the dimension of the contact area of the package lead is only 0.42mm long by 0.15mm wide.

Micro-packages are typically tested using bowl-feed type handlers with a vision system and a staging section that pre-aligns the part before being inserted into the socket. Most micro-package devices have test times shorter than one second and are tested utilizing handlers with multi-site testing capability to enhance throughput.

Testing in Matrix Format

Strip test, a method of testing devices while they are still in a matrix format on the leadframe strip, is one way to solve the socket insertion problem.

The units in strip form are held in a precise position so that the handler test-contactor alignment to the package lead can be highly accurate and repeatable compared to a singulated part.

First-pass test yields for strip-tested devices are significantly higher compared to testing parts that have been singulated and tested in pick-and-place or gravity-feed handlers.

Because the devices are in a large matrix format, strip test handlers can offer index times shorter than 0.3 seconds. Additionally, the matrix format makes it easier to test multiple devices simultaneously, which significantly improves throughput and reduces the cost of test.

Strip testing requires specially designed leadframes and lead-isolation tooling and is not a panacea; but when it makes good

Figure 4. This figure compares an end view of a SOT23 micro-package with an MSOP. (not to scale)

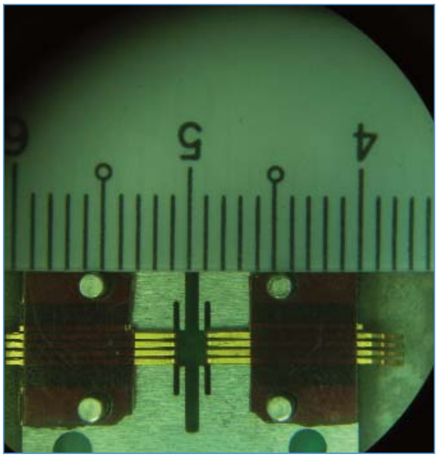

Figure 5a. A Kelvin contact test socket for an 8-lead 2x2mm MLP.

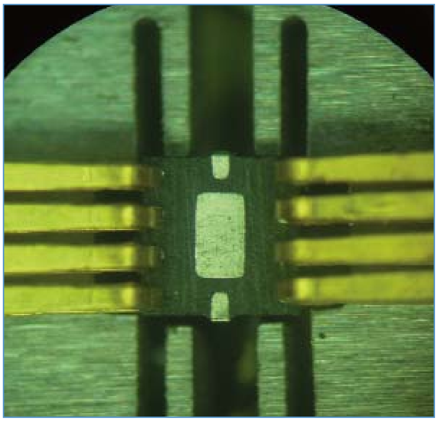

Figure 5b. This is an enlarged bottom view of the isolated two-point contactors touching the package leads.

technical and economic sense, it provides significant advantages.

Electronic Map of Good Devices

Also, by using a 2D code mark that is unique to each leadframe strip, the handler can generate an electronic "map" of the good devices, allowing the tested parts to be laser-marked prior to being singulated, as well as new data mining opportunities.

Another significant test challenge is making a Kelvin contact, which requires an isolated, two-point connection to a single lead.

For example, where the size of the package lead is only 0.42mm by 0.15mm, it is almost impossible to make a Kelvin contact using a traditional pogo pin; therefore, special sockets with cantilevered, blade-like contacts must be utilized.

Figure 5 shows a Kelvin contact test socket for an 8-lead, 2mm x 2mm MLP package and an enlarged bottom view of the contactors touching the leads of the package.

Conclusion

Many of the advanced technologies employed to make billions of leadframe-based micro-packages annually are just as challenging and "sexy" as the technologies commonly perceived as advanced technology packages.

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